

2A Li-ion Battery Switching Charger with Integrated OTG Boost

Features

- Full Automatic and Efficient Charge Management for Large Capacity Lithium Battery
 - Automatic Conditioning, CC/ CV Charge Control, Termination and Recharge
 - Support 2A Charge Current Using 33mΩ
 Sensing Resistor
 - 3MHz Synchronous PWM,1µH Low Profile Inductor
 - Input Current Regulation Accuracy: ±5% (100mA and 500mA)
 - Charge Voltage Regulation Accuracy:
 -0.25%~0.41%(25°C), ±1% (0°C to 85°C),
 ±2% (0°C to 125°C)
 - 20V Input Voltage Tolerance,
 6.3V Max Operating Voltage
 - Input Voltage Based Dynamic Power Management (VIN DPM)
 - Optional 32s/30 Minutes Safety Timer with Reset Control
 - Power Up without Battery
- Automatic Adaptor Fault Detection
- High Impedance Mode with Low Power Consumption
- Comprehensive Protection
 - Reverse Battery Leakage Protection
 - Thermal Regulation and Shut-down
 - Input & Output Over-Voltage Protection
- Built-in Input Current and Input Voltage Limit

- Automatic Charge and USB Compliant Start Sequence
- Full Range Programmable Charge Parameter through I²C Compatible Interface
 - Input Current Limit Threshold
 - Input Voltage DPM Threshold
 - Charge Termination Current
 - Charge Termination Voltage
 - Charge Termination Enable
 - Support 3.4MHz I²C HS Mode
- USB OTG Boost
 - Input Voltage Range from Battery: 2.5V~4.5V
 - 5.0V/ 400mA (V_{BAT} ≥ 3.0V)
- 3mmx3mm DFN Package

Applications

- Smart phone
- MP3 player
- Tablet PC

何业泉 销售经理15361428851 Mobile: 0755-23763432 13410664847 邮箱: hyq@szxlckj.com 深圳市信立诚科技有限公司





Order Information

| Part Number | HL7022 | | | | |
|--|--------------------|-------------------|--|--|--|
| Default Charge Termination Voltage | 4.20V | 4.20V | | | |
| OTG Mode Maximum Output Current | 400r | nA | | | |
| I ² C Address | 6AH | | | | |
| Pre-charge Current | 325mA | | | | |
| CC Current (Default) | 1050mA (Rsns=68mΩ) | 325mA (Rsns=68mΩ) | | | |
| 30min Safety Timer and 32s Watch-Dog Timer | No | Yes | | | |
| Package | DF | N | | | |
| Packing Method | Tape and Reel | | | | |
| Marking Information | HL7022FN01 | HL7022FN02 | | | |

Typical Application Diagram



Figure 2. HL7022FN02 Typical Application Diagram



| Component | Part Number | Value | Size | Vendor |
|---|--------------------|-----------|------|-----------|
| L1 | LQM2HPN1R0MGH | 1µH/2.3A | 2016 | Murata |
| Cicsp, Cicsn | C1005X5R1A104K | 0.1µF/10V | 0402 | TDK |
| Cboot | C2012X5R1E103K | 10nF/16V | 0805 | TDK |
| Cusb | C2012X5R1E105K | 1µF/25V | 0805 | ТДК |
| Cprt | C2012X5R1E475K | 4.7µF/25V | 0805 | ток |
| Cref | GRM185R61A105K | 1µF/10V | 0603 | Murata |
| Cout | GRM319R61A226ME15D | 22µF/10V | 1206 | Murata |
| Ponc | ERJ8BWFR068V | 68mΩ/1% | 1206 | PANASONIC |
| K5115 | RL0805FR-070R056L | 56mΩ/1% | 0805 | Yageo |
| R ₂₁ ,R ₂₂ | - | 1kΩ | | - |
| R ₁₁ ,R ₁₂ ,R ₂₃ ,R ₂₄ ,R ₂₅ | - | 10kΩ | | - |
| R ₁₃ | | 4.7kΩ | | |
| | | | | |

HL7022_V1.5 July. 2019



Description

HL7022 is a compact, flexible, high-efficiency, USB compliant switch-mode charge management device for single cell Li-ion and Li-polymer battery used in a wide range of portable applications. The charge parameters can be programmed through I²C interface. HL7022 integrates a synchronous PWM controller, power MOSFET, input current sensing, high-accuracy current and voltage regulation, and charge termination function into a tiny CSP package.

HL7022 provides a complete automatic three-phase battery charging control: trickle charge, constant-current charge (CC) and constant voltage charge (CV) until the battery reaches the charge termination voltage. The input current is automatically limited to the value set by the host. Charging is terminated based on the battery voltage and a

, cro cc

user selectable minimum current level. A safety timer with reset control provides a safety backup for I²C interface. During normal operation, the IC automatically restarts the charge cycle if the battery voltage falls below an internal threshold and automatically enters sleep mode or high impedance mode when the input supply is not correctly connected. The charge status can be reported to the host through the I²C interface.

During the charging process, the IC monitors its junction temperature (T_J) and reduces the charge current once T_J increases to about 120° C. To support USB OTG device, HL7022 can provide VBUS (5.0V) by boosting the battery voltage.

HL7022 is available in a 14-pin DFN package.





Pin Function





Pin Description

| | | | STAT | | | | | |
|---|------------|----------|---------------------|--|---|--|--|--|
| | | | отд | 4] HL7022 | [II] SW | | | |
| | | | ICSN | | ^[10] ₁₀ sw | | | |
| | | | VREF | 6 | PGND | | | |
| | | | CDIS | 7_] | | | | |
| | | | F | Figure 3 HI 7022 Top Vi | /iew | | | |
| | | | | | | | | |
| F | Pin Descri | ption | | | | | | |
| | PIN No. | PIN Name | I/O | | Description | | | |
| | 1 | SCL | | I ² C interface serial cl | lock. Connect SCL to 1.8V rail through a 1-10k | | | |
| | • | | | pull-up resistor. | | | | |
| | 2 | SDA | I/O | I ² C interface serial d | ata. Connect SDA to 1.8V rail through a 1-10k | | | |
| | | | | pull-up resistor. | · | | | |
| | | | | Charge status pin, op | Sen-drain. =Low when charge in progress, =HZ to | | | |
| | 3 | STAT | 0 | pin can be disabled by the EN_STAT bit in control register. STAT can be | | | | |
| | | | | used to drive an LED i | indicator or communicate with a host processor. | | | |
| | | | | HL7022FN01- Boost r | mode enable control, When OTG Pin is High, OT | | | |
| | | | $\langle O \rangle$ | enables IC to operate in boost mode. | | | | |
| | | | | HL7022FN02- Boost n | mode enable control or selection pin for input currer | | | |
| | | | | limit. | | | | |
| | 4 | OTG | | 1. When OTG mode | e is in active, OTG enables IC to operate in boos | | | |
| | | | | mode. It has higher priority over I ² C control and can be disabled using | | | | |
| | | | | the control registe | ۶r. | | | |
| | | • | | 2. After POR withou | at a host, OTG is used to select input current limi | | | |
| | | | | The input current | and threshold set by I ² C register is not used. Whe | | | |
| | χ_{O} | | | OIG=1, IINLIM=5 | 500mA; when OTG=0, IINLIM=500mA. | | | |
| | Ę | | 1 | Battery voltage and | current detection input. If there is a long trac | | | |
| | 3 | ICON | | PGND is required | tery, a ceramic capacitor (min 0.1µr) connected t | | | |
| | 6 | VRFF | 0 | Internal regulator hvo | ass output. Connect a 1uF ceramic capacitor fro | | | |
| | 5 | VINEI | 5 | internal regulator byp | alle salpat. Sonnoot a Thi Scranne sapacitor nor | | | |



| | | | this output to PGND. External load on VREF is not recommended. |
|-------|------|-----|---|
| 7 | 0010 | | Charge disable control pin. =0: charge is enabled; |
| 1 | CDIS | I | =1: charge is disabled and high impedance mode from VUSB to GND. |
| | | | Charge current sense input. Connect to the precision sense resistor in |
| 8 | ICSP | I | series with the battery. Bypass this pin with a 0.1u F ceramic capacitor to |
| | | | PGND. |
| 9 | PGND | | Power ground. |
| 10,11 | SW | 0 | Switch mode buck regulator output. |
| 40 | VDDT | 1/0 | Connection point between reverse blocking FET and high side FET. Place |
| 12 | VPRI | 1/0 | a 4.7µF ceramic capacitor from VPRT to PGND. |
| 10 | | 1/0 | Charger input voltage. Connecting a 1µF capacitor from VUSB to PGND. |
| 13 | VUSB | 1/0 | In the boost mode, it provides power to the load. |
| 1.1 | POOT | 1/0 | Connection point of bootstrap capacitor driven by High side FET. Place a |
| 14 | воот | 1/0 | 10-33nF ceramic capacitor from BOOT to SW. |
| | icc | | itan |

HL7022_V1.5 July. 2019





Internal Functional Block Diagram







Absolute Maximum Ratings⁽¹⁾

| VUSB pin voltage | 1V ~ 20V |
|---|---------------|
| VPRT, BOOT pin voltage | 0.3V ~ 20V |
| SW pin voltage : IC Not Switching | |
| IC Switching | 0.3V ~ 5.9V |
| Other pin voltage | |
| IC power, P _D @25℃ | 1,17W |
| Junction-to-ambient thermal resistance, θ_{JA} | 65℃/W |
| Junction-to-case thermal resistance, θ _{JC} | 25℃/W |
| Junction temperature, T _J | |
| Storage temperature, Tstg | |
| Pin soldering temperature, T _s (10s) | 260 °C |
| ESD: HBM | 2kV |
| ESD: CDM | 2kV |

Recommended Operating Conditions⁽²⁾

| Vue Ver SW nin Voltage | XVC | |
|--|-----|-------------|
| | | 4.5% ~ 5.5% |
| Operating free-air temperature, T _A | | |
| Junction temperature, T | | |
| | | |

Note

(1) Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device.

(2) Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied, exposure to absolute maximum rated conditions of extended periods may affect device reliability. All voltage values are with respect to the normal operation ambient temperature range is from -40°C to +85°C unless otherwise noted.



Electrical Specifications

Electrical specifications of Charge and OTG boost function

VUSB = 5 V, HZ_MODE = 0, OPA_MODE = 0 (CDIS = 0), T_A = -40°C to 125°C. And T_A=25°C unless Otherwise Noted.

| Parameter | | Test Condition | Min | Туре | Max | Unit |
|------------------|----------------------------|--|-------------------------|--------------|----------|------------|
| Input Curre | ent | | | | | 7 |
| | | VUSB > VUSB (min), PWM work | | 10 | | |
| | | V _{USB} < V _{USB (min)} , PWM Stop | | | 5 | m A |
| IUSB | VUSB CUITENT CONTROL | 0°C< T _A < 85°C, CD=1 or | | 950 | | |
| | | HZ_MODE=1 | | 000 | | μΑ |
| | | 0°C< T _A < 85°C, V _{ICSN} =4.2V | | 3 | | |
| | Battery leakage to VUSB | In High-Z mode, V _{USB} =0V, Test | | | 5 | μA |
| | | V _{USB} current | X | \mathbf{O} | | |
| l _{lgk} | In High-Z mode, battery | $0^{\circ}C < T_{A} < 85^{\circ}C$ Vicen -4.2 V In | $\langle \cdot \rangle$ | | | |
| | discharge current (input | High-Z MODE $V = 0V$ SCL SDA | | | 22 | ΠΑ |
| | from Pin ICSN, ICSP&SW | OTG = 0V or 1.8 V | | | ~~~ | μ, τ |
| | to IC) | | | | | |
| Charge Ter | mination Voltage | | | | | |
| | Output cutoff voltage | Work in cutoff voltage, | 3 50 | | <u> </u> | V |
| | setting range | programmable | 0.00 | | -1 | v |
| Voreg | | T _A = 25°C | -0.25 | | 0.41 | % |
| | Cut off voltage precision | T _J =0-85°C | -1 | | 1 | % |
| | | (Tյ =0-125°C | -2 | | 2 | % |
| Charge Cu | rrent (Fast Charge) | | | | | |
| | | Vshort ≤ Vicsn < Voreg, | | | | |
| | | R _{SNS} =68mΩ, IO_LEVEL=0, | | 1050 | | mA |
| | Low charge current (enable | OTG=High | | | | |
| | default value after 30mins | Vshort ≤ Vicsn < Voreg, | | | | |
| 1 | (mode) | R _{SNS} =68mΩ, IO_LEVEL=1, | | 325 | | mA |
| IOCHARGE | | OTG=High | | | | |
| | Cut off voltage precision | | | | | |
| | calculated through R(SNS) | | 5 | | F | 0/ |
| | (base on charge current) | | -5 | | 5 | 70 |
| У С | Vireg=Iocharge × Rsns | | | | | |
| Weak Batte | ery Detection | | | | | |
| | Weak battery voltage limit | | | | | |
| VLOWV | threshold programmable | Programmable through I ² C control | 3.4 | | 3.7 | V |
| | scale Note 1 | | | | | |



| | Weak battery voltage | | | _ | | _ | 0/ |
|-------------------|---|---|--------------------------------------|-------|------------|-------|------------|
| | accuracy | | | -5 | | 5 | % |
| | Anti peak delay of weak | Rising voltage | e, 2mV over drive, | | 20 | | |
| | battery threshold | t _{RISE} = 100 ns | | | 32 | | ms |
| CDIS & OT | G Pin Logic Level | | | | | | |
| VIL | Input low threshold level | | | | | 0.4 | |
| Vін | Input high threshold level | | | 1.2 | | . (| V |
| I _{bias} | Input bias current | Voltage on con | trol pin: 1.8 V | | | 1.0 | μA |
| Charge Ter | mination Detection | | | | | | |
| | The termination charging | VICSN> VOREG - | V _{RCH} , | 50 | 5 | 400 | ~ ^ |
| | current programmable range | R _{SNS} =68 mΩ, p | orogrammable | 50 | | 400 | mA |
| | Anti peak delay of termination | The rise and | fall,2mV overdrive, | | | | m 0 |
| Iterm | charge | trise, tfall = 10 | 0 ns | | 3 2 | | ms |
| | Through R _{SNS} termination | 3.4 mV ≤V(IREG | _term) ≤ 6.8 mV | -20 | | 20 | |
| | current adjust accuracy | $6.8 \text{ mV} < V_{(IREC)}$ | _{G_TERM)} ≤ 17 mV | -10 | | 10 | % |
| | V_{IREG} term = Iterm × Rsns | 17mV <vireg_te< td=""><td>-5.5</td><td></td><td>5.5</td><td></td></vireg_te<> | -5.5 | | 5.5 | | |
| Adapter De | tection | | | | | | |
| | Input voltage limit(min) | Adapter detect | 3.8 | 4 | 4.2 | V | |
| | Anti peak delay when VUSB | Rising voltage, | | 22 | | me | |
| VUSB (min) | rise to $V_{\text{USB (min)}}$ | t _{RISE} = 100 ns | | | 52 | | 1115 |
| | VUSB (min) hysteresis | Input voltage ri | sing | | 200 | | mV |
| LUOD DETEOT | From the current source to | During the dete | oction of adaptor | | 50 | | m۸ |
| IUSB_DETECT | the GND | Duning the dete | ection of adapter | | 50 | | |
| tint | Detection time interval | The input powe | er detection | | 2 | | S |
| Input Base | d on Dynamic Power Managem | nent | | | | | |
| | The input voltage DPM | | | | | | |
| Vuon now | threshold programmable | | | 4.213 | | 4.773 | V |
| V 05B_DPM | range | | | | | | |
| • | V _{USB_DPM} threshold accuracy | | | -2 | | 2 | % |
| Input Curre | ent Limit | | | | | | |
| | The input current limit | I _{IN} = 100mA | $T_A = 0^{\circ}C \sim 125^{\circ}C$ | 86 | 93 | 100 | mA |
| | threshold | $I_{IN} = 500 \text{mA}$ | $T_A = 0^{\circ}C \sim 125^{\circ}C$ | 450 | 475 | 500 | mA |
| VREF Inter | nal Bias Reference Comparato | r | | | | | |
| Vorr | Internal bias voltage | VUSB>VUSBN(min) | ,Ivref=1mA, | 20 | | 5.0 | V |
| VKEF | reference | C _{VREF} =4.7µF | 5.0 | | 5.9 | v | |
| The Battery | <pre>/ Recharge Threshold</pre> | | | | | | |



| VRCH | Recharge threshold voltage | Below Voreg | 100 | 120 | 150 | mV |
|--|--|--|-----|-----|--------------|-----|
| | Anti peak delay | V_{ICSN} reduce below threshold, t_{FALL} =100ns, 10mV overdrive | | 128 | | ms |
| The State of | of Output | | | | | |
| | Low level output saturation voltage, STAT pin | Io = 10 mA, sink current | | | 0.4 | N |
| VOL(STAT) | STAT High level leakage current | STAT pin voltage :5.5 V | | | 1 | μΑ |
| I ² C Bus Log | gic Level& Timing | | | , C | (0) | |
| Vol | The output of low threshold level | Io = 10 mA, sink current | | | 0.4 | V |
| VIL | Input low threshold level | V _{pull-up} = 1.8 V, SDA & SCL | 5 |), | 0.4 | V |
| VIH | Input high threshold level | V _{pull-up} = 1.8 V, SDA & SCL | 1.2 | | | V |
| BIAS | input bias current | Vpull-up = 1.8 V, SDA & SCL | | | 1 | μA |
| fsc∟ | SCL clock frequency | | | | 3.4 | MHz |
| Battery Det | tection | | | | | |
| Idetect | The battery detection current, before the charging is completed (sink current) | Start after terminated detection, V _{ICSN} ≤ V _{OREG} | | 0.9 | | mA |
| tdetect | Battery detection time | | | 350 | | ms |
| Sleep Mode | e Parameters | | | 1 | | |
| VSLP | Sleep-mode threshold V _{USB} V _{ICSN} | 1.3 V ≤ V _{ICSN} ≤ V _{OREG} , V _{USB} declining | | -60 | | mV |
| | Sleep-mode Exit hysteresis | $2.3 \text{ V} \leq \text{V}_{\text{ICSN}} \leq \text{V}_{\text{OREG}}$ | | 135 | | mV |
| VSLP_EXIT | V _{USB} rise to V _{SLP} + V _{SLP_EXIT} Anti peak delay | Rising voltage, 2mV overdrive, t _{RISE} = 100 ns | | 32 | | ms |
| PWM | | | | | | |
| Voltage bet | ween BOOT pin & SW pin | During charging or boosting period | | | 6.5 | V |
| Q1: The inp | ut FET conduction resistance | I _{IN_LIMIT} = 500 mA, Measure between V _{USB} and V _{PRT} | | 130 | | |
| QU: The high -side FET conduction resistance | | Measure between SW and V _{PRT} , $V_{BOOT} - V_{SW} = 4V$ | | 100 | | mΩ |
| QD: The low-side FET conduction | | Measure between SW and PGND | | 96 | | |
| | Oscillator frequency | | | 3.0 | | MH7 |
| fosc | Frequency accuracy | | -10 | | 10 | % |



| - - | | | | | <u> 1L7</u> | <u>'022</u> |
|--|--|--|-----|-----|-------------|-------------|
| D _{MAX} | Max duty cycle | | | 98 | | |
| D _{MIN} | Min duty cycle | | 0 | | | |
| Charge Mo | de Protection | | | | | |
| Vovp_in_usb | V _{USB} OVP threshold voltage | V _{BUS} reach threshold during charge period and turn off converter | 6.1 | 6.3 | 6.5 | v |
| | Vovp_IN_USB hysteresis | Vuse fall down to Vovp_in_use | | 200 | | mV |
| Ilimit | During charging, cycle by cycle current limit | Work in charge mode | | 2.2 | | A |
| VSHORT | Short circuit charge cycle voltage threshold | V _(ICSN) rise | 1.9 | 2.0 | 2.1 | V |
| | V _{SHORT} hysteresis | V(ICSN) fall below VSHORT | | 100 | • | mV |
| ISHORT | The trickle charge current | V(ICSN) ≤ VSHORT | 20 | 30 | 40 | mA |
| Boost Mode | e (OPA_MODE = 1, HZ_MODE | = 0) | | | | |
| | Output voltage (to V _{USB} pin) | 2.5V < V(ICSN) < 4.5 V | | 5.0 | | V |
| Vusb_b | Output voltage accuracy | Including the line and load regulation | -3 | | 3 | % |
| Іво | Max output current | 3.0 V < V(ICSN) < 4.5 V | | 400 | | mA |
| IBLIMIT | Cycle current limit | 2.5 V < V(ICSN) < 4.5 V | | 2.2 | | А |
| VUSBOVP | Overvoltage protection threshold (V _{USB} pin) | If boosting period threshold exceed V _{USB} , shut down converter | 6.1 | 6.3 | 6.5 | V |
| | VUSBOVP hysteresis | Vuse turn down from Vusbovp | | 200 | | mV |
| | | In boosting period | | 2.5 | | V |
| VBATMIN | Min battery voltage (Icsn pin) | Ahead of Boost start | 2.8 | 2.9 | 3.0 | V |
| Protection | \mathcal{C} | | | | | |
| Т | Over temperature protection | | | 145 | | |
| I SHTDWN | Temperature hysteresis | | | 20 | | °C |
| Тсғ | Over temperature current | Charges current start to decline | | 120 | | 0 |
| t325 | 32 seconds watchdog timer | 32 seconds mode or HOST mode | 15 | 32 | | S |
| t _{30M} | 30 minutes safety timer | 30 minutes mode | 15 | 30 | | min |

Table 3. Electrical Specifications

Note:

(1) In 30 minutes mode of HL7022, if the battery is charged to a higher voltage than the termination voltage, charger will enter Hi-Z mode and wait for the I²C command.



Typical Characteristics

 $V_{USB} = 5 \text{ V}, V_{BAT} = 3.6 \text{ V}, I_{OCHARGE} = 1450 \text{mA}, T_A = 25^{\circ}\text{C}$ unless otherwise noted.







Figure 11. Battery Removal/ Insertion During Charging









Figure 14. Boost PFM Waveform (IUSB=50mA)



Figure 16. Boost mode load transient (IUSB=500mA->0mA)



HL7022 provides complete automatic three-phase battery charging and management: constant pre-charge, high current switching- mode constant current (CC) charge and constant voltage (CV) charge until the battery voltage rises to the termination voltage. When the battery voltage drops below the internal threshold limit, the IC will automatically restart a charging cycle. If the input power supply is disconnected, the IC will automatically enter the high-Z mode to prevent the battery from being dissipated. When the IC's temperature rises to 120 °C, it will automatically reduce the charging current to prevent the IC from overheating.

HL7022 has three operation modes: charge mode, boost mode and high-Z mode. In the charge mode, the IC supports a single lithium-ion battery or lithium-polymer battery to be accurately charged. In the boost mode, the IC will boost the battery voltage and provide power to the OTG device connected to the VUSB pin. In the high-Z mode, the IC stops operation and enters high impedance state. In this state, the current consumption from the VUSB terminal and from the battery terminal is minimized. When the handheld device is in standby state, this mode can effectively reduce the IC power consumption.

The host communicates through I²C (HOST mode or 32 seconds mode) to control the IC to operate in different modes. If the I²C host is absent, The IC will start the 30-minute safety timer and enter the 30-minute (default) mode, in which the charger will continue charging the battery using default register value and charging parameters until the safety timer times out. After that, the charger stops and enter HZ mode.

IC Operation in Charge Mode

When a good battery with voltage below recharge threshold limit is inserted, and a good adapter is detected,

HL7022 enters the charge mode. In this mode the IC has 5 control loops to regulate the input voltage, input current, charging current, charging voltage and IC temperature.

HL7022

During the charging period, all 5 loops are enabled and one of them is in control. Figure 17(a) shows a typical charging curve without inputting current regulation loop. This is a standard Li-Ion battery CC/CV charging curve. Figure 17 (b) shows in the CC mode, a typical charging curve with the IC's input current is limited.

In a switched-mode charger like HL7022, the charge current is higher than the input current; therefore the charging process will be faster than the traditional linear charge scheme. In HL7022, input voltage limit threshold of the dynamic power management (DPM) loop, input current, charge current, termination current and termination voltage etc. can all be set by the I²C interface.



Figure 17(a). Typical charging curve without input current limit





Figure 17(b). Charging curve with input current limit

PWM Controller in Charge Mode

HL7022 provides a highly efficient synchronous 3MHz PWM controller to regulate the charging current and voltage. Power MOSFETS are also integrated. Its duty cycle ranges from 0% to 95%.

HL7022 has three NMOS power MOSFET: input reverse-blocking FET Q1, high- side FET QU and lowside FET QD. When V_{USB} is lower than V_{ICSN} , Q1 prevents battery from discharging to V_{USB} . A charge pump circuit is used to provide gate drive for Q1, while a bootstrap circuit with an external bootstrap capacitor is used to supply the gate drive of Q2.

Cycle-by-cycle (CBC) current limit is implemented in QU for safe operation and output short-circuit protection.

Battery Charge Process

When the battery voltage is lower than $V_{(SHORT)}$ threshold, the IC provides a trickle current $I_{(SHORT)}$ to the battery. When the battery voltage rises to between V_{SHORT} and V_{OREG} , The charger enters CC phase by increasing charge current to quick charge current $I_{OCHARGE}$, or a value matching the input current limit I_{IN_LIM} if that threshold is reached.

Built-in soft-start scheme slowly increases the quick

charge current to its target value to minimize current and voltage overshoot on the battery. Both the input current limit IIN_LIMIT and quick charge current IOCHARGE can be set by the host. Once the battery voltage reaches the regulation voltage VOREG, the charger enters CV phase, and the charge current tapers down as shown in Figure 4. Regulation of the voltage loop is based on monitoring the voltage between ICSN and PGND and compare against an internal reference voltage. In HOST mode, the regulation voltage is set between 3.54V to 4.48V. In 30-minute mode, the regulation voltage is fixed at 4.2V.

During the CV phase, HL7022 also monitors the charge current. In HOST mode with charge termination enabled (TE=1), the IC will turn off charging if ICSN pin voltage is higher than the battery recharge threshold VOREG-VRCH for more than 32 ms (typical), and measured charge current is less than the termination charge current ITERM. At this time, IC will turn on a discharge current IDETECT on ICSN pin for tDETECT (typical 256ms), then check the battery voltage. If the battery voltage is still higher than the recharge threshold after tDETECT, the battery charging is complete. The battery detection routine is used to ensure charge termination does not occur because the battery is removed. The STAT bits and STAT pin are updated to indicate charge completion. The host can program charge termination current level, as well as disabling charge termination function by setting termination bit (TE) to 0.

A new charge cycle is initiated when one of the following conditions is detected:

- The battery voltage falls below the VOREG VRCH threshold.
- VBUS Power-on reset (POR), if battery voltage is below the V_(LOWV) threshold.
- Bit of \overline{CE} toggles or RESET bit is set (under Host control)



Operation in Boost mode

In 32-second mode, the host can enable HL7022's boost mode operation through one of the following two methods:

1. Set OTG_EN=1, OTG_PL=1(default), then set OTG pin=1. Or set OTG_EN=1, OTG_PL=0, then set OTG pin=0;

2. Set OPA_Mode =1

In boost mode, the IC provides 5V output to the USB port. The maximum output current can reach 400mA (I_{BO}) when battery voltage is 3.0V or higher.

PWM Controller in Boost Mode

Similar to the charge mode, HL7022 provides an integrated PWM controller in boost mode to regulate VUSB pin voltage. CBC current limit of 1.6A on the low-side power MOSFET QD provides output overload and short-circuit protection.

Boost Start-Up and Protection

HL7022 has built-in boost soft start sequence to prevent battery in-rush current and inductor current saturation. The IC also provides battery under-voltage, output over-voltage and chip over-temperature protection.

Boost PFM Mode

Under light load conditions, the IC operates in PFM mode to reduce the power loss and maintain converter efficiency. During boosting, the PWM converter is turned off once the inductor current is less than 0mA, and the PWM will start switching only when VSUB voltage drops below output target voltage. HL7022 automatically switches between PWM and PFM mode depending on load conditions.

Safety Timer in Boost Mode

At the beginning of boost operation, the IC starts a

32-second timer. It is reset by the host using the I²C interface.

Writing "1" to reset bit of TMR_RST in control register will reset the 32-second timer and TMR_RST is automatically set to "0" after the 32 second timer is reset. Once the 32-second timer expires, the IC exits the boost mode, enables the fault pulse on the STAT pin and sets fault status bit in the status register. The fault condition is cleared by POR or host control.

HIGH IMPEDANCE (Hi-Z) MODE

In Hi-Z mode, the charger stops charging and enters a low quiescent current state to conserve power. The chip enters High-Z mode if one of the following conditions are met.

1. Set CDIS pin =1.

 In 30-minute mode and CDIS pin=0: VBUS > VBUS (min) and battery present with V_{BAT}> VLOWV.

3 In host mode, CDIS pin=0, OTG_EN=0: set HZ_MODE bit =1.

If HL7022 enters High-Z state in 30-minute mode, CDIS pin=0, and the battery voltage V_{BAT} < $V_{(LOWV)}$, the 32-second timer is activated to wait for the host control. Once the 32-second timer expires, the IC re-enters 30 minute mode and 32-second timer is disabled.

If HL7022 enters HiZ state in host mode, CDIS pin=0, and $V_{BUS} > V_{BUS(min)}$, IC can exit Hi-Z mode by writing "0" to the HZ-MODE control bit.

In the 30-minute mode, set CDIS pin=1 resets the 30-minute timer.

Other Functions

HL7022 has comprehensive fault reports. Please refer to the Application Information section for detailed description.



Serial Interface Description

I²C is a 2 wire serial interface. The bus consists of a data line (SDA) and a clock line (SCL) with a pull-up device. When the bus is idle, both SDA and SCL lines are pulled high. All I²C compatible devices connect to the I²C SDA and SCL buses through open drain I/O pins. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific condition that indicates the START and STOP of data transfer. A slave device receives and /or transmits data on the bus under control of the master device.

HL7022 works as a slave and is compatible with the following data transfer modes as defined in the I²C Bus Specification: Standard mode (100kbps), Fast mode (400kbps), Fast mode plus (1000kbps) and High-speed mode (up to 3.4Mbps in write mode). The interface adds flexibility to the battery charge solution by making most functions and parameters programmable through the I²C host.

The data transfer protocol for Standard mode, Fast mode and Fast mode plus is the same, therefore referred to as F/S mode in this document. The protocol for High-speed mode is different and referred to as HS-mode.

F/S Mode Protocol

The master initiates data transfer by generating a START condition. The START condition is when a high-to-low transition occurs on the SDA line while SCL is high. The master stops data transfer by generating a STOP condition, in which a low-to-high transition occurs on the SDA line while SCL is high. This is shown in Figure 18.



HL702

After START condition, the master generates SCL pulse, and transmits 7-bit slave address and the read/write bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 19.)



Figure 19. Bit Transfer on the Serial Interface

All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 20) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge signal, the master knows that communication link with a slave has been established.



Figure 20. Acknowledge on the I²C Bus

The master generates further SCL cycles to either transmit data to the slave (R/W bit =1) or receive data



from the slave (R/W bit =0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a STOP condition (see Figure 21). This releases the bus and stops the communication link with the addressed slave.

All I²C compatible devices must recognize the STOP condition. Upon receiving the STOP condition, all devices know that the bus is released, and they wait for a start byte followed by a matching address. If a transmission is terminated prematurely, the master needs to send a STOP condition to prevent the slave I²C logic from getting stuck in a bad state. Attempting to read data from register addresses not listed in this section will



H/S Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The master generates a START byte followed by a valid serial byte containing HS master code 0000 1XXX. This transmission is made in F/S-mode with speed less than

1Mbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4Mbps operation.

The master then generates a Repeated Start condition (a Repeated START condition has the same timing as the start condition). After this Repeated START condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4Mbps are allowed. A STOP condition ends the H/S mode and switches all the internal settings of the slave devices to support F/S mode. Instead of using a STOP condition, repeated start conditions should be used to secure the bus in HS mode. If a transmission is terminated in advance, the master needs sending a STOP condition to prevent the slave I²C logic from getting stuck in a bad state.

Attempting to read data from register addresses not listed in this section will result in FFh being read out.

I²C Update Sequence

The IC requires a START condition, a valid I²C address, a register address byte, and a data byte for a single update. After receiving of each byte, the IC sends acknowledge by pulling the SDA line low during the high period of a single clock. A valid I²C address will selects this IC. The IC performs an update on the falling edge of the acknowledge signal that follows the LSB bit.

For the first update, the IC requires a START condition, a valid I²C address, a register address byte and a data byte. For all consecutive updates, the IC needs a register address byte and a data byte. Once a STOP condition is received, the IC releases the I²C bus and waits for a new START condition.



| ymm ymm ymm i i i i i < | S SLAVE ADDRESS R/W A REGISTER ADDRESS A DATA AA | Slave | Addre | ess By | te | | | | |
|--|--|-----------------------|--------------------------|---------------------------|----------------------------|----------------------------|---------------------------|---------|---|
| □ find the state of the state | 0' (Write) Data Transferred Data Transferred Data Transferred Data Transferred | MSB | | | | | | LSE | 5 |
| In the slave address byte is the first byte received following the START condition from the master device. Figure 22. Data Transfer Format in F/S(H/S) mode In the slave address byte is the first byte received following the START condition from the master device. | From master to IC A = Acknowledge (SDA LOW) A = Not Acknowledge (SDA HIGH) From IC to master S = \$TART condition | 1 | 1 | 0 | 1 | 0 | 1 | 0 | Х |
| gister Description | <complex-block><figure></figure></complex-block> | 1 The sl the ST | 1 Iave add FART co | 0 dress by ondition | 1 /te is the from th | 0 e first by e maste | 1 yte rece er devic | 0 e. | X |
| | gister Description | | | | | | | | |

Register Description

| r | | | | | | | | | |
|--------------|-------------|---|--------------|---|---|---|---|---|---|
| Register | | | Address Bits | | | | | | |
| Name | Hex Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHG_STATUS | 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CHG_CONTROL0 | 01Н | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| OREG | 02H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| IC_INFO | 03H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| IBAT | 04H | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| CHG_CONTROL1 | 05H | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| SAFETY | 06H | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| MONITOR0 | 10H | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

Table 4. Register map of HL7022



Bit Definitions

The following table defines the operation of each register bit. Bold font indicates power-on default values.

| Bit | Name | Value | Туре | Function | | | |
|----------|-----------------------------|-------------------------|---|--|--|--|--|
| | CHG_STATUS | 6 | Re | egister Address: 00 Default Value:X1XX 0XXX | | | |
| TMD DQT/ | | | Write 1 reset watchdog timer (automatic clearar | | natic clearance); write "0" has no | | |
| 7 | | 1 | vv | effect | | | |
| | 010 | | R | Return the OTG pin status (1=high) | | | |
| 6 | EN STAT | 0 | | Disable the STAT pin function | | | |
| 0 | EN_STAT | 1 | K/VV | Enable the STAT pin function | | | |
| | | 00 | | Ready | | | |
| 5.4 | STAT. | 01 | Б | Allow PWM charging. If CE=0, char | ging. | | |
| 5.4 | STAT | 10 | ĸ | Charge termination | | | |
| | | 11 | | Function egister Address: 00 Default Value:X1XX 0XXX Write 1 reset watchdog timer (automatic clearance); write "0" ha effect Return the OTG pin status (1=high) Disable the STAT pin function Enable the STAT pin function Ready Allow PWM charging. If CE=0, charging. Charge termination Fault (fault status) IC is not in BOOST mode IC is in BOOST mode IC is in BOOST mode IC is in BOOST mode Boost soft start failure Poor Input Source VBAT VIN OVP Battery OVP Thermal Shutdown Thermal Shutdown Timer Fault Timer Fault; reset all regist No Battery N/A ter Address: 01 Default Value:0011 0000-HL7022FN02 100mA 500mA 800mA USB host limit for input cur No limit for input current-HL7022FN01 3.4V 3.5V 3.6V 3.7V Disable charge termination function | | | |
| 2 | POOST | 0 | Р | IC is not in BOOST mode | | | |
| 3 | 60031 | 1 | ĸ | IC is in BOOST mode | | | |
| | | | | Charge mode | Boost mode | | |
| | | 000 | | pe Function Register Address: 00 Default Value:X1XX 0XXX V Write 1 reset watchdog timer (automatic clearance); write "0" has he effect Return the OTG pin status (1=high) Disable the STAT pin function W Enable the STAT pin function Ready Allow PWM charging. If CE=0, charging. Charge termination Fault (fault status) IC is not in BOOST mode Charge mode IC is in BOOST mode Boost mode Normal (No Fault) Normal (No Fault) VIN OVP VIN OVP Sleep Mode Boost soft start failure Poor Input Source VEAT-CUVLOBST Output OVP Battery OVP Thermal Shutdown Thermal Shutdown Timer Fault Timer Fault; reset all registers No Battery N/A gister Address: 01 Default Value:0011 0000-HL7022FN02 100mA 500mA 800mA USB host limit for input current No limit for input GistV 3.6V 3.6V 3.6V 3.6V Brable charge termination function | Normal (No Fault) | | |
| | | 001 | | | VIN OVP | | |
| | | 010 | | Sleep Mode | Boost soft start failure | | |
| 2:0 | FAULT | 011 | R | Poor Input Source | Boost soft start failure V _{BAT} <uvlobst< td=""></uvlobst<> | | |
| | | 100 | C. | Output OVP | Battery OVP | | |
| | | 101 Thermal Shutdown Th | Thermal Shutdown | | | | |
| | | 110 | \sim | Timer Fault | Timer Fault; reset all registers | | |
| | | 111 | $\mathbf{\mathcal{S}}$ | No Battery | N/A | | |
| (| CHG_CONTROL0 | | Registe | r Address: 01 Default Va | alue:0011 0000-HL7022FN02 | | |
| | | 00 | | 100mA | | | |
| | . () | 01 | | 500mA | | | |
| 7:6 | | 10 | R/W | 800mA | USB host limit for input current | | |
| | $\mathcal{O}_{\mathcal{V}}$ | 11 | | No limit for input | | | |
| | | 11 | | current-HL7022FN01 | | | |
| | \mathcal{O} | 00 | | 3.4V | | | |
| 5.4 | Views | 01 | R/M | 3.5V | Weak battery threshold | | |
| 0.4 | V LOWV | 10 | 17/17 | 3.6V | | | |
| | | 11 | | 3.7V | | | |
| 3 | ТЕ | 0 | ₽ ^// | Disable charge termination funct | ion | | |
| 3 | IE | 1 | 11/11 | Enable charge termination function | -HL7022FN01 | | |
| 2 | CE | 0 | R/W | Enable charge function | | | |



| | | 4 | | Dischler | was from the | | | | |
|-----|-------------|-----|------------|-------------------------------|----------------------|--------------|------------------------------|---------------------|-------------------------|
| | | 1 | | Disable charge function | | | | | |
| 1 | HZ_MODE | 0 | R/W | Disable High-Z mode | | | | | |
| | | 1 | | Enable High-Z mode | | | | | |
| 0 | OPA_MODE | 0 | | Charge mode | | | | | |
| | | 1 | | Boost mode | Э | | | | |
| | OREG | | Regis | ter Address: | 02 | Default | Value:1000 1 | 110 | $\overline{\mathbf{O}}$ |
| | | | | Charge | e termination Def | voltage, pro | ogrammable e 00011 (4.20V | every step 20 ′) | JmV. |
| | | | | HEX | Voreg | HEX | | HEX | Voreg |
| | | | | 00 | 3.50 | 10 | 3.82 | 20 | 4.14 |
| | | | | 01 | 3.52 | 11 | 3.84 | 21 | 4.16 |
| | | | | 02 | 3.54 | 12 | 3.86 | 22 | 4.18 |
| | | | | 03 | 3.56 | 13 | 3.88 | 23 | 4.20 |
| | | | | 04 | 3.58 | 14 | 3.90 | 24 | 4.22 |
| | | | | 05 | 3.60 | 15 | 3.92 | 25 | 4.24 |
| 7:2 | OREG | | R/W | 06 | 3.62 | 16 | 3.94 | 26 | 4.26 |
| | | | | 07 • | 3.64 | 17 | 3.96 | 27 | 4.28 |
| | | | | 08 | 3.66 | 18 | 3.98 | 28 | 4.30 |
| | | | | 09 | 3.68 | 19 | 4.00 | 29 | 4.32 |
| | | | | 0A | 3.70 | 1A | 4.02 | 2A | 4.34 |
| | | | | OВ | 3.72 | 1B | 4.04 | 2B | 4.36 |
| | | | | 0C | 3.74 | 1C | 4.06 | 2C | 4.38 |
| | | | | 0D | 3.76 | 1D | 4.08 | 2D | 4.40 |
| | | | | 0E | 3.78 | 1E | 4.10 | 2E | 4.42 |
| | | | | 0F | 3.80 | 1F | 4.12 | 2F~3F | 4.44 |
| 1 | | 0 | R/\/ | OTG pin Lo | w valid | | | | |
| | | 1 | 1 1/ 7 1 | OTG pin H | igh valid | | | | |
| 0 | | 0 | R/\/ | In host mode, disable OTG pin | | | | | |
| | | 1 | | In host mod | de, Enable O | TG pin | | | |
| | IC_INFO | | Regis | ster Address: | 03 | Default | Value:010X X | XXX | |
| 7:5 | Vendor Code | 010 | R | This IC ve | ndor numbe | r | | | |
| 4:3 | PN | | R | Part Numbe | er | | | | |
| | | | | IC version. | | | | | |
| 2:0 | REV | | R | 010, IO_LE | VEL=0, HL7 | 022FN01; | | | |
| | | | | 011, IO_LE | VEL=1, HL7 | 022FN02. | | | |
| | IBAT | R | egister Ad | dress: 04 | Default | t Value:0000 | 0001-HL702 | 22FN02 | |
| 7 | RESET | 0 | R/W | Writing 0 h | as no effect | t.(Note: rea | d always retu | urns 1) | |



| | | 1 | | Reset all registers except Safety re | gister (Reg6) | | | | |
|--------------|---------------|-----|-------|--|---|--|--|--|--|
| | | | | Note: Rsns=68 mΩ | Note: Rsns=56 mΩ | | | | |
| | | 000 | | 550mA | 667mA | | | | |
| | | 001 | 001 | 750mA | 789mA | | | | |
| | | 010 | | 850mA | 910mA | | | | |
| | | 011 | | 950mA | 1032mA | | | | |
| 6:4 | IOCHARGE | 100 | R/W | 1050mA-HL7022FN01 | 1275mA-HL7022FN01 | | | | |
| | | 101 | | 1150mA | 1396mA | | | | |
| | | 110 | | 1350mA | 1639mA | | | | |
| | | 111 | | 1450mA | 1760mA | | | | |
| 3 | Reserved | 0 | R/W | N/A | × (2) | | | | |
| | | 000 | | 50mA | | | | | |
| | | 001 | | 100mA | | | | | |
| | | 010 | | 150mA | Note: Rsns=56 mΩ 667mA 789mA 910mA 1032mA 1275mA-HL7022FN01 1396mA 1639mA 1639mA 1639mA 1639mA 1032mA 1032mA 1275mA-HL7022FN01 1396mA 1639mA 1639mA 1639mA 100mA 100mA 100mA 100mA 100mA Note: Rsns=56 mΩ Note: Rsns=56 mΩ 100mA 1032mA 11275mA-HL7022FN01 1039mA 1039mA 1030mA 1030mA 1031ma 10100ma A er IOCHARGE. Ove voltage limit threshold) threshold) VIN loop control threshold | | | | |
| | _ | 011 | | 200mA | | | | | |
| 2:0 | Iterm | 100 | R/W | 250mA | Charge termination current | | | | |
| | | 101 | | 300mA | - | | | | |
| | | 110 | | 350mA | - | | | | |
| | | 111 | | 400mA | - | | | | |
| CHG_CONTROL1 | | | | Register Address: 05 Defa | ult Value:001X X100 | | | | |
| 7:6 | NA | | R/W | N | A | | | | |
| F | | 0 | DAW | Charge current controlled by registe | er IOCHARGE. | | | | |
| Э | IO_LEVEL | 1 | R/VV | Charge current fixed at 325mA. | | | | | |
| 4 | SD. | 0 | J | VIN loop not in control (VIN still abo | ove voltage limit threshold) | | | | |
| 4 | 58 | | ĸ | VIN loop in control (VIN within limit | threshold) | | | | |
| 0 | | 0 | P | CDIS is high | | | | | |
| 3 | EN_LEVEL | 0 | ĸ | CDIS is low | | | | | |
| | | 000 | | 4.213V | | | | | |
| | \mathcal{A} | 001 | | 4.293V | | | | | |
| | \cap | 010 | | 4.373V | | | | | |
| | | 011 | D 44/ | 4.453V | | | | | |
| 2:0 | VSP | 100 | K/VV | 4.533V | vin loop control threshold | | | | |
| | | 101 | 1 | 4.613V | 1 | | | | |
| • | | 110 | | 4.693V | 1 | | | | |
| | | 111 | 1 | 4.773V | 1 | | | | |
| | SAFETY | / | Re | egister Address: 06 Default V | alue:0100 0000 | | | | |





| | 7 | Reserved | 0 | R | | | |
|---|---------|------------|--------------|--------|--|--------------------------------|--|
| | | | 000 | | 550mA | | |
| | | | 001 | | 750mA | | |
| | | | 010 | | 850mA | Set the maximum Charge current | |
| | 6.1 | | 011 | | 950mA | IOCHARGE. Default value 0100 | |
| | 0.4 | ISAFE | 100 | r/vv | 1050mA | (1050mA). | |
| | | | 101 | | 1150mA | | |
| | | | 110 | | 1350mA | | |
| | | | 111 | | 1450mA | | |
| | | | 0000 | | 4.20V | | |
| | | | 0001 | | 4.22V | | |
| | | | 0010 | | 4.24V | | |
| | | | 0011 | | 4.26V | | |
| | | VSAFE | 0100 | | 4.28V | | |
| | | | 0101 | | 4.30V | | |
| | 2.0 | | 0110 | | 4.32V | Set the maximum battery | |
| | 3.0 | | 0111 | | 4.34V | voltage. | |
| | | | 1000 | | 4.36V | | |
| | | | 1001 | | 4.38V | | |
| | | | 1010 | • | 4.40V | | |
| | | | 1011 | C. | 4.42V | | |
| | | | 1100 | \sim | | | |
| | | | ~1111 | | 4.44 V | | |
| | | MONITOR | | Re | egister Address: 10 Default V | /alue: XXXX XXXX | |
| | 7 | ITERM_CMP | | R | ITERM comparator output. 1 means | s ICHARGE>ITERM | |
| | 6 | VBAT_CMP | \mathbf{O} | R | VBAT comparator output. 1 means V | usb>Vicsn | |
| | 5 | LINCHG | | R | 30mA linear charge status. 1 means linear charge running. | | |
| | 4 | T 120 | | D | 120°C Over temperature protection. | | |
| | 4 1_120 | | | IX. | When T_120=1 and T_145=0, charge current will be limited. | | |
| | 3 | ICHG | | R | 0 indicates ICHARGE loop is controlling charge current. | | |
| | 2 | IVUSB | | R | 0 indicates IUSB loop (input current) is controlling charge current. | | |
| | 1 | VUSB_VALID | | R | 1 indicates VUSB can be use to cha | arge after detection. | |
| N | 0 | CV | | R | 1 indicates Constant Voltage loop is | s in control of charging. | |

Table 5. Register map of HL7022. Bold characters indicate default values upon POR.



Application Information

Interrupt (STAT Pin) Description

STAT is a open-drain output pin. It drives a pull-up resistor and informs the host of HL7022 working status. In normal conditions its output is high. In fault conditions, a 128-µs pulse is sent to notify the host.

| Status | STAT Pin | | | |
|----------------------------|--------------------|--|--|--|
| Charge & EN_STAT=1 | LOW | | | |
| Other normal conditions | OPEN | | | |
| Charge mode fault: | | | | |
| Timer fault, Sleep Mode, | 100 up pulse then | | | |
| VUSB/VBAT OVP, VUSB UVLO, | | | | |
| Poor input source, Battery | OPEN | | | |
| absent, Thermal shutdown | | | | |
| Boost mode fault: | | | | |
| Timer fault, Over load, | 128-µs pulse, then | | | |
| VUSB/VBAT OVP, VBAT UVLO, | OPEN | | | |
| Thermal shutdown | | | | |

Table 6. STAT Signal

Over Temperature Limit and Protection

In the charging process, in order to prevent the IC from overheating, HL7022 will monitor its junction temperature T_J to prevent the IC from overheating. Once the temperature reaches the thermal limit threshold T_{CF}, the IC will reduce the charging current. If T_J has reached T_{SHTDWN}, the IC will suspend charging. Under this thermal-protection mode, the PWM controller will shut down and all timers freeze. When T_J drops below T_{SHTDWN} by about 20°C, the IC resumes charging.

USB Plug-In

Before the USB power is plugged in, the I²C host can keep writing 1 to TMR_RST so the chip stays in host mode. Once USB power is plugged in, HL7022 will enter normal charge mode using parameters from the register set. If the IC is not in host mode when USB power is plugged in, IC will work in 30-minute mode, in which the IC will charging for 30 minutes with default charging parameters, until the host communicates with the IC.

The default values of the registers are set at low level of charging current and termination voltage. This prevents violation of USB specification or over-charging any type of lithium- ion batteries. At the same time the termination voltage is set high enough to prevent the I²C host from losing power supply.

Termination Current Sensing Resistor Selection Guidelines

The termination current depend on the external sensing resistor (R_{SNS}). The termination current step (IOTERM_STEP) can be calculated using Equation 1:

$$IO(TERM_STEP) = \frac{VI(TERM0)}{R(SNS)}$$
(1)

Table 7 shows the setup of termination current for three sensing resistors.

For example, with a $68m\Omega$ sense resistor,

V(ITERM2)=1,V(ITERM1)=0,and V(ITERM0)=1,then ITERM =

[(13.6mV x 1) + (6.8mV x 0) + (3.4mV x 1) + 3.4mV]/

 $68m\Omega = 200mA + 0 + 50mA + 50mA = 300mA$.

| | V | I _(TERM) | I _(TERM) | I _(TERM) | I(TERM) |
|-----------|----------------------------------|---------------------|---------------------|---------------------|---------------|
| ріт | v I _(TERM) (mV) | (mA) | (mA) | (mA) | (mA) |
| DIT | | $R_{(SNS)} =$ | $R_{(SNS)} =$ | $R_{(SNS)} =$ | $R_{(SNS)} =$ |
| | | 33mΩ | 56mΩ | 68mΩ | 100mΩ |
| VI(TERM2) | 13.6 | 412 | 242 | 200 | 136 |
| VI(TERM1) | 6.8 | 206 | 124 | 100 | 68 |
| VI(TERM0) | 3.4 | 103 | 61 | 50 | 34 |
| Offset | 3.4 | 103 | 61 | 50 | 34 |

Table 7. Termination Current Setting

Output Inductor and Capacitance Selection Guidelines





HL7022 provides full internal loop compensation. With the internal loop compensation, the highest stability occurs when the LC resonant frequency fo, is approximately 40 kHz (20 kHz to 80 kHz). Equation 2 can be used to calculate the value of the output inductor L_{OUT} , and output capacitor C_{OUT} .

fo =
$$\frac{1}{2\pi\sqrt{LOUT \times COUT}}$$
 (2)

To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 22 μ F and 100 μ F is recommended for C_{OUT}.

Soldering

Following Profile is suggested for standard Pb-Free soldering process. A unique reflow profile may be required for each assembly depends on the solder paste applied. Please adhere to recommendations of solder paste manufacturer. Reflow oven temperature profiles should be characterized using an accurate thermal thermal mass, and should be confirmed at all critical component location (exposed lands) on the board using a shielded thermocouple.

| Profile Feature | Pb-Free Assembly |
|--|---|
| Preheat/Soak Temperature Min(T _{smin}) Temperature Max(T _{smax}) Time(t _s) from (T _{smin} to T _{smax}) | 150°C 200°C 60-120 seconds |
| Ramp-up rate (T_L to T_p) | 3°C /second max |
| Liquidous temperature (TL) Time(tL) maintained above TL | 217°C 60-150 seconds |
| Peak package body temperature (T _P) | The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds. |
| Time(t _p)* within 5°C of the specified classification temperature (T _c), see Figure 23. | 30* seconds |
| Ramp-down rate $(T_p \text{ to } T_L)$ | 6°C /second max |
| Time 25°C to peak temperature | 8 minutes max |

 Table 8 Standard Pb-Free Soldering Profile





PCB Layout Reference

PCB layout is important to optimal HL7022 performance .The following provides some guidelines:

(1) To obtain optimal performance, the power input capacitors, connected from power input to PGND, should be placed as close to the IC as possible. The output inductor should be placed close to the IC and the output capacitor connected between the inductor and PGND of the IC. The intention is to minimize the current path loop area (from the SW pin through the LC filter to the PGND pin and back to IC). To prevent high frequency oscillation problem, use proper layout to minimize high frequency current path loop. The sense resistor should be close to the junction of the output capacitor and inductor. The sense path must connect to the underneath of the resistor, and do not cross any high-current path.

(2) Place all decoupling capacitors close to their respective IC pins and close to PGND. Do not place components on any high-current path. All small control signals should be kept away from any high current path.

(3) The PCB should have a dedicated ground plane, which is connected to all components through via holes (two via holes per power-stage capacitors; two via holes for the IC PGND; one via per capacitor of small-signal components). Use star connection to separate different parts (high-power/low-power/small-signal) of the application design to reduce coupling noise and ground noise. Using small-size layout and independent ground connection will reduce ground noise and minimize coupling between signals.

(4) The high-current charge paths of VBUS, PMID, SW and PGND pins must be sized appropriately according to

their maximum charge current in order to minimize voltage drops on their PCB routes. The PGND trace carry the return current from the internal low-side power FET, and should also be connected to the ground plane.

(5) Place the 4.7μF input capacitor as close to VPRT and PGND pins as possible to minimize high frequency input current loop area. Place the VUSB capacitor as close to VBUS and PGND pins as possible for the same reason.



Figure 24. High Frequency Current Path





Package Information



NOTE:

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.



Tape and Reel Information



| Device | Package | SPQ | Reel Diameter (mm) | Tape Width (mm) | A0 | B0 | K0 | PIN1 |
|--------|---------|------|--------------------|-----------------|-----------|-----------|-----------|------|
| HL7022 | DFN-14 | 1500 | 330±2 | 12±0.3 | 4.30±0.10 | 4.30±0.10 | 1.10±0.10 | Q1 |



Important Notice

Halo Micro reserves the right to modify, improve and terminate its products, service, documentation, etc. without advance notice. Customers are encouraged to contact Halo Micro sales representative get the latest product information.

Without proper legal authorization, Halo Micro products shall not be used for medical or military applications. Halo Micro does not assume any liability of personal or property damages of any kind due to such applications.

All text, images, trademarks of this document, and any intellectual property contained in the product and in this document belong to Halo Micro No part of this document may be used, copied, modified, distributed or published without legal authorization from Halo Micro.

> 何业泉 销售经理15361428851 Mobile: 0755-23763432 13410664847 邮箱: hyq@szxlckj.com 深圳市信立诚科技有限公司